REMARKS

This is in response to the Office Action mailed January 23, 2006. In the Office Action, (i) the drawings were objected; (ii) the Abstract was objected; (iii) the Title was objected; (iv) the Cross Reference Section was objected; (v) Claims 55-57 were objected; and Claims 20-24 and 40-57 were rejected under 35 U.S.C. § 102(b). Reexamination and reconsideration of this case is respectfully requested in view of the amendments made herein and the following remarks.

Claims 22, 50 and 55-57 have been amended by this response. Claims 1-19 and 25-39 and were previously cancelled. No claim has been added or cancelled by this response. Claims 20-24 and 40-57 remain at issue in the patent application. Of those remaining at issue, claims 20, 40, 45, and 50 are independent claims.

Applicant believes that no new matter has been added by this response.

I) OBJECTION OF THE DRAWINGS

On page 2 of the Office Action, the drawings were objected for failing to comply with 37 CFR 1.84(i) & 37 CFR 1.84(p).

There was no specific objection to any figure made by the Office Action.

Applicant herewith transmits the formal drawings under separate cover. It is believed that this objection is now moot and its withdrawal is respectfully requested.

II) OBJECTION OF THE SPECIFICATION

On page 2 of the Office Action, the abstract, title, and cross reference section were objected.

Applicant has amended the title to "BUS STATE KEEPERS" as suggested in the Office Action.

Applicant has amended the Cross-Reference to Related Applications section, on page 1, line 4. The paragraph thereat has been amended to update the status of the cross-noted applications to which this divisional patent application claims the benefit thereof.

Applicant has amended the abstract.

Applicant believes these objections are now moot and respectfully requests their withdrawal.

III) CLAIM OBJECTIONS

On page 2 of the Office Action, claims 55-57 were objected. Specifically, claims 55-57 were objected due to the fact that on line 2 of each, "the first bus" appears to be "the output bus".

Applicant has amended dependent claims 55-57 to correct the informality. Applicant believes this objection is now moot and respectfully requests its withdrawal.

IV) CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

On pages 3-5 of the Office Action, claims 20-24 and 40-57 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent

5,396,130 issued to Galbraith et al. ("Galbraith"). Applicant respectfully traverses this rejection.

Note that independent claims 40, 45, and 50 were not specifically addressed by the Office Action. Instead, the Office Action generally rejected these independent claims stating "Claims 40, 41, and 43 are essentially the same in scope as apparatus claims 20-24 and are rejected similarly" and "Claims 45-52 are essentially the same in scope as apparatus claims 20-44 and are rejected similarly."

Regarding independent claim 20, the Office Action alleges "Galbraith discloses, in Figs, 1-4, a bus state keeper comprising:

a plurality (since there are N-hits) of multiplexers (MUX 16; see Fig. 2) each having

a select input (MODE), a first input (output of 14), a second input (20A), and an output (16A), the output coupled to each respective bit of a first bus (16A) coupled to a plurality of devices (directly and indirectly to 18,20, 14, and 17), wherein the first bus is to he kept in a steady state when inactive (when 20A is selected by MODE),

the first input coupled to each respective hit of a second bus (output of 14),

the select input of each of the plurality of multiplexers coupled to a select signal (MODE); and

a plurality of flip flops (see 18,20) each having a data input (DI), a data output (20A) and a clock input (CI), the data input coupled to each respective bit of the first bus (16A),

the data output coupled respectively to the second input of the plurality of multiplexers, the clock input coupled to a clock signal (CI; see col. 5, lines 10+),

the plurality of flip flops (18, 20) to store a state (col. 3, lines 67+) of the first bus in response to the select signal (MODE)."

Applicant respectfully disagrees.

The Office Action seems to be alleging that the output of Galbraith's fuse sensing circuit 14 is Applicant's second bus. However, Applicant has diligently searched Galbraith for the word "bus" and no such word is found therein.

Galbraith's output from Galbraith's fuse sensing circuit 14 is not a bus. Galbraith's Figure 2 illustrates Galbraith's sensing circuit 14 and Galbraith's multiplexer circuit 16. Galbraith's sensing circuit 14 has an internal fuse sense state node coupled to the gates of transistors 46,48 of Galbraith's multiplexer circuit 16.

Additionally, the logical setting on the node of Galbraith's sensing circuit 14 is fixed by Galbraith's fuse 12A or Galbraith's zener 12B. That is, the node of Galbraith's sensing circuit 14 does not change state or float as a bus driven by a tristate driver can. Galbraith's "sensed state of fuse 12A is either a logic low or 0 when the fuse is intact or a logic high or 1 after the fuse is blown or modified to an open circuit. When the shorting device zener 12B is used, the sensed state of the zener 12B is either a logic high or 1 when the zener is intact or a logic low or 0 after the zener is zapped or modified to a short circuit." [Galbraith, Col. 4, lines 44-50].

The Office Action further seems to be allege that Galbraith's MODE signal is Applicant's select signal and that Galbraith's N-Bit Load Shift Register 18 and N-Bit Holding Register with Trim Override Values 20 "store a state of the first bus in response to the select signal (MODE)." However, Galbraith's N-Bit Load Shift Register 18 and N-Bit Holding Register with Trim Override Values 20 are not controlled by Galbraith's MODE signal.

As illustrated in Galbraith's FIG. 1, a "PARALLEL LOAD SIGNAL" and "OUT OF PHASE CLOCKS FOR SERIAL LOAD" are coupled into Galbraith's N-Bit Load Shift Register 18. A "LOAD REGISTER" signal is coupled into Galbraith's N-Bit Holding Register with Trim Override Values 20. These signals differ from Galbraith's MODE signal that is coupled into Galbraith's muxtiplexer 16. Thus, Galbraith does not disclose a "plurality of flip flops to store a state of the first bus in response to the select signal" as is recited in Applicant's independent claim 1.

Additionally, Galbraith's N-Bit Load Shift Register 18 and N-Bit Holding Register with Trim Override Values 20 do not appear to store a state of Galbraith's line 16A, as is otherwise alleged by the Office Action.

Galbraith's "mode control logic input of shift register 18 labelled PARALLEL LOAD selects the parallel load input for feedback of the trim word at line 16A output of the multiplexer 16. The trim word feedback allows a ***first stored trim state to be modified.***" (sic) [Galbraith, Col. 3, line 68 - Col. 4, line 5] Galbraith's "[h]olding register 20 applies the ***override signal*** or

sequential ***different trim values*** to the multiplexer 16." (Emphasis Added) [Galbraith, Col. 4, lines 10-12]

For the foregoing reasons, Applicant respectfully submits Galbraith does not anticipate or make obvious Applicants independent claim 20.

As the Office Action similarly rejected independent claims 40, 45 and 50, Applicant respectfully submits that independent claims 40, 45 and 50 are also not anticipated nor made obvious by Galbraith.

Claims 21-24, 41-44, 46-49 and 51-52 depend directly or indirectly from independent claims 20, 40, 45 and 50 respectively. As Applicant believes it has placed the independent claims in condition for allowance, dependent claims with additional limitations are also believed to be in condition for allowance.

Accordingly, Applicant respectfully requests the Examiner to withdraw the outstanding §102(b) rejection of claims 21-24, 41-44, 46-49 and 51-57 by Galbraith.

V) CLAIM AMENDMENTS

Applicant has amended claims 22, 50, 55-57.

Claims 55-57 were amended to overcome the claim objections as discussed previously.

Claim 22 was amended to delete an instance of "from the plurality of multiplexers" to be consistent with the second "outputting" element in the claim.

Claim 50 was amended to clarify that it is "the respective bit" of the output bus that is coupled to a plurality of devices.

Thus, claims 22 and 50 were amended to clarify Applicant's claimed invention and not for reasons related to patentability.

CONCLUSION

In view of the foregoing it is respectfully submitted that the pending claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,
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Dated: July 24, 2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 *on:* July 24, 2006.

Tu T. Nguyen 7/24/06
Date